TITLE: INTEGRATED PRESSURE SENSOR FOR MEASURING MULTI-AXIS PRESSURE GRADIENTS

TECHNICAL FIELD

The present invention generally relates to semiconductor processing, and in particular to a system and method for characterizing chemical mechanical polishing (CMP) processes *via* wafer-based electrical resistance member(s) and/or electrical resistance entities.

BACKGROUND

As semiconductors have become more complicated (*e.g.,* increasing number of interconnect layers), the planarization of dielectric and metal layers has become more important to achieving desired critical dimensions (CDs) in such semiconductors. One technique employed in the planarization of layers is chemical mechanical polishing (CMP). In general, CMP is a surface planarization technique in which a wafer is processed by a polishing pad in the presence of an abrasive slurry (although recent slurry-free techniques are also employed). One goal of CMP is more global planarization with stricter planarization tolerances and more repeatable results. In CMP, high elevation features are selectively removed resulting in a topology with improved planarity. Such removal is achieved, at least in part, *via* a combination of a chemical process and an abrasive process.

Some goals of CMP include achieving satisfactory planarity across a wafer, achieving desired film thickness uniformity, removing chemical reaction products and/or layers at a desired rate, achieving desired selectivity and/or endpoint detection and to not introduce defects into a wafer undergoing CMP. Whether these goals are achieved can depend on a variety of factors. Removal rate may depend, for example, on the type of material being removed, the relative velocity between the wafer and the abrasive pad, the temperature of the wafer, the slurry feed rate, the type of polishing motion employed, the slurry formula, the slurry pH, the concentration of solids in the slurry, slurry particle size, pad hardness and pad conditioning.

The mechanics of metal CMP include chemically forming an oxide of the metal on the metal film surface on the wafer. The oxide is then removed mechanically *via,* for example, abrasives in the slurry. The mechanics of other CMP

(*e.g.*, polysilicon polish, dielectric polish) similarly involve a chemical reaction followed by a mechanical removal of reaction products.

The polishing pad facilitates precisely removing reaction products at the wafer interface to facilitate precise layer thickness production. For example, CMP processes can be employed to precisely remove around 0.5 to 1.0 μm of material. The polishing pads may vary, for example, in hardness and density. For example, pads can be relatively stiff or relatively flexible. A less stiff pad will conform more easily to the topography of a wafer and thus while reducing planarity may facilitate faster removal of material in down areas. Conversely, a stiffer/less flexible pad may produce better planarity but may result in slower removal in down areas. The degree to which the pad conforms to the topography can affect the friction between the pad, slurry and wafer. Furthermore, the polishing pads may glaze during processing of wafers, which again may affect the abrasiveness and thus heat generated by friction during CMP. For example, a new pad may achieve a removal rate of around 210 nm/min while a pad that has been employed to polish fifty wafers may only achieve a removal rate of around 75 nm/min. Thus, the rate at which CMP progresses may vary depending on, for example, the hardness, density and glazing of the pad employed.

The rate at which CMP progresses may also vary depending on parameters of the slurry employed. Slurries may consist, for example, of small abrasive particles suspended in a solution (*e.g.*, aqueous solution). Acids or bases can be added to such solutions to facilitate, for example, the oxidation of the metal on the wafer and/or other chemical reactions involved in other non-metal CMP processes. Slurry parameters that may impact polishing rates include, but are not limited to, the chemical composition of the slurry, the concentration of solids in the slurry, the solid particles in the slurry and the temperature of the wafer to which the slurry is applied.

Conventional CMP processes have either lacked control systems, requiring pre-calculated CMP parameters based on theoretical or indirect empirical data, or have had indirect control, which is based on indirect information. Such pre-determined, theoretical and/or indirect measurement based parameters do not provide adequate initialization and/or monitoring and thus do not facilitate precise characterization and/or control of the CMP process.

Fabricating an integrated circuit (IC) typically includes sequentially depositing conducting, semiconducting and/or insulating layers on a silicon wafer. One

fabrication step includes depositing a metal layer over previous layers and planarizing the metal layer. For example, trenches or holes in an insulating layer may be filled with a conducting metal. After CMP planarization, portions of the conductive metal remaining between the raised pattern of an insulating layer may form, for example, vias, plugs and/or lines. The precision with which such vias, plugs and/or lines can be formed affects the achievable CDs for an IC, and thus improvements in characterizing and/or controlling a CMP process are desired.

SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an extensive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts of the invention in a simplified form as a prelude to the more detailed description presented later.

The present invention provides a system and method that facilitates characterizing and/or controlling a chemical mechanical polishing (CMP) process by gathering wafer stress information during CMP processing, where the wafer stress(es) are determined from electrical resistance member(s) and/or electrical resistance entities in the wafer. Thus, accuracy improvements over conventional systems that only indirectly measure wafer stress(es) (*e.g.*, defect(s)) by measuring the pressure of an abrasive pad may be achieved. The system includes wafer-based electrical resistance member(s) and/or entities and apparatus to determine wafer stress(es) from such wafer-based electrical resistance member(s) and/or entities.

One example of the system further includes a data store that can be employed to store data including, but not limited to, electrical resistance information, slurry information, wafer information, motion (*e.g.*, rotary, orbital, linear) information, and abrasive pad information associated with the CMP process being characterized. Another example of the system further includes a CMP control system that can be employed to analyze such wafer stress, slurry, wafer, pressure, motion, and/or pad information to facilitate characterizing a CMP process, to facilitate selecting CMP process parameters and/or for controlling, *in-situ*, a CMP process.

The present invention thus provides a technique to monitor electrical resistance(s) of electrical resistance member(s) and/or electrical resistance entities in a wafer during CMP processing. The present invention can be employed in CMP processing of metal films including, but not limited to, copper (Cu), tantalum (Ta), gold (Au), tungsten (W), aluminum (Al) and titanium (Ti), and alloys thereof, for example. The present invention can also be employed in CMP processing of layers including, but not limited to, polysilicon layers and dielectric layers. To facilitate retrieving wafer electrical resistance(s), the substrate may include signal processing circuitry, a power source, and other components, for example. The monitored electrical resistance information can be used to determine wafer stress(es).

In another example of the present invention, the system includes a wafer that has a metal layer and/or substrate and electrical resistance member(s) and/or electrical resistance entities located in and/or on the metal layer and/or a substrate. The system also includes a electrical resistance monitoring system that can read the wafer electrical resistance(s) from the electrical resistance member(s) and/or electrical resistance entities and determine wafer stress(es) to characterize the CMP process. Characterizing the CMP process includes producing information concerning factors including, but not limited to, polishing rate, polishing uniformity and introduction of defects during polishing. The factors can be correlated, for example, with polishing parameters including, but not limited to, polishing time, polishing temperature, polishing pressure, polishing speed, slurry properties and wafer/metal layer properties as related to wafer stress information. For example, rotation speed, pressure and removal rate may be identifiable by stress(es) of the wafer. Such characterization can be employed, for example, to facilitate initializing subsequent chemical mechanical polishing processes and/or apparatus and/or to control such chemical mechanical polishing processes and/or apparatus.

To the accomplishment of the foregoing and related ends, the invention, then, comprises the features hereinafter fully described and particularly pointed out in the claims. The following description and the drawings set forth in detail certain illustrative embodiments of the invention. These embodiments are indicative, however of but a few of the various ways in which the principles of the invention may be employed. Other objects, advantages and novel features of the invention will

become apparent from the following detailed description of the invention when considered in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a wafer with associated electrical resistance members in accordance with an aspect of the present invention.

Fig. 2 illustrates a wafer with associated electrical resistance members in two directions in accordance with an aspect of the present invention.

Fig. 3 illustrates a wafer with associated electrical resistance members in three directions in accordance with an aspect of the present invention.

Fig. 4 illustrates a wafer with a layer and a substrate associated with various configurations of electrical resistance members in accordance with an aspect of the present invention.

Fig. 5 illustrates a wafer with associated electrical resistance members in accordance with an aspect of the present invention.

Fig. 6 is a block diagram of a CMP characterizing system, in accordance with an aspect of the present invention.

Fig. 7 is a block diagram of a CMP characterizing and controlling system, in accordance with an aspect of the present invention.

Fig. 8 illustrates one example CMP system.

Fig. 9 illustrates an example CMP process.

Fig. 10 is a flow diagram illustrating an example methodology for characterizing and/or controlling a CMP process, in accordance with an aspect of the present invention.

Fig. 11 is a flow diagram illustrating an example methodology for programming a CMP process based, at least in part, on CMP characterization data, in accordance with an aspect of the present invention.

Fig. 12 illustrates a wafer with features and electrical resistance members in accordance with an aspect of the present invention.

Fig. 13 is a flow diagram illustrating an example methodology for monitoring and/or controlling a CMP process based, at least in part, on CMP characterization data, in accordance with an aspect of the present invention.

DETAILED DESCRIPTION

The present invention will now be described with reference to the drawings, where like reference numerals are used to refer to like elements throughout. The following detailed description is of the best modes presently contemplated by the inventors for practicing the invention. It should be understood that the description of these aspects are merely illustrative and that they should not be taken in a limiting sense.

Referring to Fig. 1, a wafer 100 with a first electrical resistance member(s) 110 in accordance with an aspect of the present invention is illustrated. The wafer 100 may include one or more substrate layers (*e.g.*, monocrystalline silicon, SiO_2), one or more conducting layers (*e.g.*, metal), one or more semiconducting layers and one or more insulating layers, for example. Semiconductor wafer composition and fabrication techniques are well known in the art and thus are omitted for the sake of brevity. However, conventional wafers have not typically included electrical resistance members for use in CMP.

The first electrical resistance member(s) 110 can be located in and/or on the polysilicon layers, metal layers, the dielectric layers and/or the substrate layers and can be electrically isolated in one or more of these layer(s). The first electrical resistance member(s) 110 are oriented in a first direction (*e.g.*, x). In the instance where the first electrical resistance member(s) 110 are located in and/or adjacent to metal layer(s), the first electrical resistance member(s) 110 can be electrically isolated (*e.g.*, insulated) from the metal layer(s).

The first electrical resistance member(s) 110 have an associated electrical resistance which changes with a stress (*e.g.*, mechanical) change in the first direction (*e.g.*, piezoresistive change). For example, the first electrical resistance member(s) 110 can comprise a semiconductor material such as doped amorphous or polycrystalline silicon. Additionally, the first electrical resistance member(s) 110 can be a resistive polymer. The associated electrical resistance can be used, for example, by a system (not shown) to determine wafer stress.

Turning next to Fig. 2, a wafer 200 with electrical resistance members in two directions in accordance with an aspect of the present invention. The wafer 200 includes first electrical resistance member(s) 110 and second electrical resistance member(s) 120. The wafer 200 may include one or more substrate layers (*e.g.*, SiO_2),

one or more conducting layers (*e.g.*, metal), one or more semiconducting layers and one or more insulating layers, for example.

The first electrical resistance member(s) 110 and/or the second electrical resistance members(s) 120 can be located in and/or on the polysilicon layers, metal layers, the dielectric layers and/or the substrate layers and can be electrically isolated in one or more of these layer(s). The first electrical resistance member(s) 110 are oriented in a first direction (*e.g.*, x) while the second electrical resistance member(s) 120 are oriented in a second direction (*e.g.*, y). For example, the first electrical resistance member(s) 110 can be substantially orthogonal to the second electrical resistance member(s) 120. Further, the first electrical resistance member(s) 110 can be electrically (*e.g.*, conductively) coupled to the second electrical resistance member(s) 120 – forming an electrical resistance entity 122. The second electric resistance member(s) 120 have an associated electrical resistance which changes with a stress (*e.g.*, mechanical) change in the second direction (*e.g.*, piezoresistive change). In the instance where the second electrical resistance member(s) 120 are located in and/or adjacent to metal layer(s), the second electrical resistance member(s) 120 can be electrically isolated (*e.g.*, insulated) from the metal layer(s).

Next, referring to Fig. 3, a wafer 300 with electrical resistance members in three directions in accordance with an aspect of the present invention. The wafer 300 includes first electrical resistance member(s) 110, second electrical resistance member(s) 120 and third electrical resistance member(s) 130. The wafer 200 may include one or more substrate layers (*e.g.*, SiO_2), one or more conducting layers (*e.g.*, metal), one or more semiconducting layers and one or more insulating layers, for example.

The first electrical resistance member(s) 110, the second electrical resistance members(s) 120 and/or the third electrical resistance member(s) 130 can be located in and/or on the polysilicon layers, metal layers, the dielectric layers and/or the substrate layers and can be electrically isolated in one or more of these layer(s). The first electrical resistance member(s) 110 are oriented in a first direction (*e.g.*, x), the second electrical resistance member(s) 120 are oriented in a second direction (*e.g.*, y) and the third electrical resistance member(s) 130 are oriented in a third direction (*e.g.*, z). For example, the first electrical resistance member(s) 110 can be substantially orthogonal to the second electrical resistance member(s) 120. Further, the first electrical

resistance member(s) 110 and the second electrical resistance member(s) can be substantially orthogonal to the third electrical resistance member(s) 130. In the instance where the third electrical resistance member(s) 130 are located in and/or adjacent to metal layer(s), the third electrical resistance member(s) 130 can be electrically isolated (*e.g.*, insulated) from the metal layer(s).

The first electrical resistance member(s) 110 can be electrically (*e.g.*, conductively) coupled to the second electrical resistance member(s) 120 and/or the third electrical resistance member(s) 130 – forming an electrical resistance entity 124. The third electrical resistance member(s) 130 can have an associated electrical resistance which changes with a stress (*e.g.*, mechanical) change in the third direction (*e.g.*, piezoresistive change).

While Fig. 3 illustrates a wafer 300 that includes a plurality of first electrical resistance member(s) 110, second electrical resistance member(s) 120, and third electrical resistance member(s) 130, it is to be appreciated that single first electrical resistance member(s) 110, second electrical resistance member(s) 120, and/or third electrical resistance member(s) 130 may be employed with the present invention. The first electrical resistance member(s) 110, second electrical resistance member(s) 120, third electrical resistance member(s) 130, and/or combination(s) thereof may be arranged on the wafer 300 in various schemes. For example, in Fig. 3, the electrical resistance members 110, 120, 130 are arranged in a random pattern. Other arrangements may include, but are not limited to, broken and unbroken linear, circular, ellipsoidal, sinusoidal, hyperbolic, parabolic and wave arrangements. Furthermore, the electrical resistance members 110, 120, 130 may be arranged according to a matrix and/or a pattern, for example. It is to be appreciated that various patterns may be employed to facilitate characterizing various CMP properties.

Turning to Fig. 4, a wafer with a layer 410 and a substrate 420 associated with various configurations of electrical resistance entity in accordance with an aspect of the present invention. A first electrical resistance entity 430 is illustrated as being positioned on the layer 410 while a second electrical resistance entity 440 is illustrated as being positioned above and in the layer 410 and a third electrical resistance entity 450 is illustrated as being positioned in both the layer 410 and the substrate layer 420.

The first electrical resistance entity 430, the second electrical resistance entity 440 and/or the third electrical resistance entity 450 can comprise electrical resistance

member(s) oriented in one, two and/or three directions. Thus, the first electrical resistance entity 430, the second electrical resistance entity 440, and/or the third electrical resistance entity 450 can have associated electrical resistance(s) which change with stress change(s) in one, two and/or three direction(s) (*e.g.*, piezoresistance change(s)).

While Fig. 4 illustrates three electrical resistance entity locations, it is to be appreciated that a wafer 400 may be fabricated with a greater and/or lesser number of electrical resistance entities and that other electrical resistance entity locations can be employed in accordance with the present invention. It is to be further appreciated that electrical resistance entities may be employed in various type of layers including, but not limited to, metal, polysilicon layers and dielectric layers.

Thus, Fig. 5 presents a top view and a cross section view of a wafer 500. The wafer 500 has two rings of electrical resistance entities 510, 520. The first ring 510 is comprised of individual electrical resistance entities 512 placed at a substantially uniform depth within a layer 530 of the wafer 500. The second ring 520 is comprised of individual electrical resistance entities 514 distributed at different levels throughout the layer 530 and a substrate layer 540.

While Fig. 5 illustrates a possible arrangement and depth distribution, it is to be appreciated that other arrangements and depth distributions can be employed in accordance with the present invention. Furthermore, while Fig. 5 illustrates electrical resistance entities in a wafer, it is to be appreciated that other electrical resistance-related equipment (*e.g.*, signal processing circuitry, power source, electrical resistance processor *etc.*) may be incorporated onto and/or into a wafer in accordance with the present invention to facilitate reading electrical resistance data from electrical resistance entities associated with a wafer. Furthermore, while Fig. 5 does not illustrate IC features fabricated into and/or onto a wafer, it is to be appreciated that such features may co-exist with the electrical resistance entities and/or electrical resistance-related equipment.

Turning now to Fig. 6, a block diagram of a CMP characterizing and controlling system 600 is illustrated. The CMP characterizing system 600 a wafer 610 that includes one or more electrical resistance member(s) and/or electrical resistance entities as described above, a CMP system 620 and a data store 640.

The system 600 may be employed, for example, to characterize and/or control a CMP process. Thus, during a characterizing only phase, the wafer 610 may be a test wafer (*e.g.,* contains only electrical resistance member(s), electrical resistance entities and/or electrical resistance related equipment) but during a characterizing and/or fabrication phase, the wafer 610 may be a production wafer incorporating IC features, electrical resistance member(s), electrical resistance entities and/or electrical resistance-relating equipment. Such features may include, but are not limited to, vias, plugs, lines and the like. The test wafer may be made of the same materials as a wafer requiring CMP processing to enable one to tailor the CMP process specifically to the wafers requiring CMP processing.

The system 600 includes an electrical resistance monitoring system 630 that can be employed to gather electrical resistance information including, but not limited to, the electrical resistance of electrical resistance member(s) and/or entities embedded in the wafer 610 before the CMP process, electrical resistance(s) recorded during the chemical mechanical polishing process and the time associated with such reading, electrical resistance(s) recorded after revolutions of a polishing pad during the chemical mechanical polishing process and the number of revolutions associated with such reading, and electrical resistance(s) recorded after one or more percentages of the layers have been removed during the chemical mechanical polishing process and the percentage removed associated with such reading. Based at least in part upon the electrical resistance(s), the electrical resistance monitoring system 630 can determine associated wafer stress(es).

As CMP progresses, various electrical resistance(s) may be monitored. The sequence in which such electrical resistance(s) are generated can be analyzed to determine the rate at which CMP is progressing and also to predict times when CMP may be substantially completed and/or times when an *ex-situ* quality control analysis may be appropriate. Furthermore, such a sequence of electrical resistance(s) may be employed to predict, for example, when subsequent processes are to be scheduled and/or when an abrasive pad should be replaced or conditioned.

For example, at a first point in time T1, an electrical resistance signature S1 may have been produced, which indicates that electrical resistance(s) readings should be taken at a second point in time T2 and a third point in time T3 and that it is likely that the CMP process may terminate at a time T4. Thus, at the second point in time

T2 an electrical resistance signature S2 may be recorded and at a third point in time T3 an electrical resistance signature S3 may be recorded. Furthermore, equipment required for the semiconductor processing of the wafer 610 may be scheduled for T4.

Analyzing the sequence of signatures, and the time required to produce transitions between such signatures can facilitate determining whether CMP is progressing at an acceptable rate, can facilitate predicting optimal times to pause a CMP process to probe the process and can facilitate determining when CMP should be terminated. Feedback information can be generated from such sequence analysis to maintain, increase and/or decrease the rate at which CMP progresses. For example, one or more slurry formulae and/or concentrations can be altered to affect the CMP rate based on the signature sequence analysis. Feed forward information can be generated to facilitate configuring subsequent fabrication processes. For example, feed forward control data employed in apparatus scheduling and/or initialization may be generated and fed forward to one or more processes and/or apparatus. It is to be appreciated that various aspects of the present invention may employ technologies associated with facilitating unconstrained optimization and/or minimization of error costs. Thus, non-linear training systems/methodologies (*e.g.,* back propagation, Bayesian, fuzzy sets, non-linear regression), or other neural networking paradigms including mixture of experts, cerebella model arithmetic computer (CMACS), radial basis functions, directed search networks and function link networks may be employed.

The system 600 includes a data store 640 that can be employed to store the electrical resistance data, and other information (*e.g.,* pad, slurry, pressure, motion) and relationship data. Such data can be stored in data structures including, but not limited to one or more lists, arrays, tables, databases (relational, hierarchical), stacks, heaps, linked lists and data cubes. Furthermore, the data can be stored in manners to facilitate processing like on line analytical processing (OLAP), data mining and online process control (OPC). The data can reside on one physical device and/or may be distributed between two or more physical devices (*e.g.,* disk drives, tape drives, memory units). Analyses associated with the data stored in the data store 640 can be employed to control one or more CMP parameters (*e.g.,* formula, components, concentration, time, pressure, material being polished, rotation speed) and in the present invention can be employed to terminate and/or pause CMP, for example.

In one example of the present invention, the electrical resistance monitoring system 630 includes a relater that can be employed to produce relations between information including, but not limited to, wafer information, electrical resistance information, pad information, slurry information, pressure information and motion information, for example. Such relations may be stored, for example, in the data store 640. Such relations may be stored, for example, in a relational database record, a hierarchical database record, an OLAP record, a data cube dimension record, an object and the like. The relater may be, for example, a computer component. As used in this application, the term "component" is intended to refer to a computer-related entity, either hardware, a combination of hardware and software, software, or software in execution. For example, a component may be, but is not limited to being, a process running on a processor, a processor, an object, an executable, a thread of execution, a program, and a computer. By way of illustration, both an application running on a server and the server can be a component.

As illustrated in Fig. 7, the system 600 can, optionally, include a CMP control system 650 that can be employed to analyze electrical resistance information, other information (*e.g.,* temperature, pad, pressure, wafer, slurry, motion) and relations between such information to control the CMP system 620. By way of illustration, if desired electrical resistance(s) (*e.g.,* associated wafer stress(es)) have been achieved, then the CMP control system 650 may maintain the CMP parameters. By way of further illustration, if desired electrical resistance(s) (*e.g.,* associated wafer stress(es)) have not been achieved, (*e.g.,* surface defect(s) causing stress on electrical resistance member(s)), then the CMP control system 650 may adjust one or more CMP parameters (*e.g.,* slurry dispense rate, pressure) to facilitate achieving such a desired result. More precise control can be employed to facilitate optimizing, for example, the chemical reaction (*e.g.,* oxidation) employed in CMP and thus more precise CMP processes can be achieved, providing advantages over conventional systems.

In one example of the present invention, the CMP control system 650 may include an initializer that can be employed, for example, to initialize the CMP system 620 and/or a CMP process based on CMP characterization data. The initializer may be, for example, a computer component. Such initialization may be based, at least in part, on characterization data retrieved from the data store 640, the electrical resistance monitoring system 630 and/or the CMP system 620. For example, when

the CMP system 620 is presented with a wafer 610 with known characteristics (*e.g.*, layer type, thickness, initial planarity, desired planarity, *etc.*), the CMP control system 650 may configure parameter(s) including, but not limited to, one or more pressures (*e.g.*, initial, average, maximum, minimum) at which the CMP system 620 should operate, the speed (*e.g.*, initial, average, maximum, minimum) at which the CMP system 720 should operate, slurry parameters (*e.g.*, formula, pH, concentration, particle density, particle size, *etc.*) and pad parameters (*e.g.*, use current pad, get different pad, *etc.*). Thus, the CMP control system 650 can be employed to facilitate establishing initial parameters for the CMP system 620, which facilitates producing a desired CMP process (*e.g.*, desired removal rate, desired defect level, desired planarity, desired uniformity) that can be monitored *via* the wafer 610 based electrical resistance member(s) and/or electrical resistance entities.

In another example of the present invention, the CMP control system further includes a controller that can be employed, *in-situ*, to update one or more CMP parameters (*e.g.*, pressure, speed, slurry properties) to facilitate producing a higher quality CMP. Such *in-situ* control may be based, for example, on electric resistance(s) read from the wafer 610 during CMP, where the electrical resistance(s) are correlated with the characterization data stored, for example, in the data store 640. The controller may be, for example, a computer component.

Fig. 8 illustrates one example CMP system 800. Such systems are well known in the art and thus are only briefly discussed herein. The system 800 includes a rotating platen 810 upon which a polishing pad 820 has been placed. A slurry dispenser 840 is employed to dispense a layer of slurry 830 onto the polishing pad 820. A wafer 850, upon which a chemical reaction (*e.g.*, oxidation, hydrolysis) is and/or has occurred is maneuvered by a wafer carrier 860 to be brought in contact with the slurry 830 and/or the abrasive pad 820 to facilitate removing the reaction products. While a slurry system is illustrated, it is to be appreciated that the present invention can be employed in accordance with non-slurry systems. It is to be further appreciated that while a rotary system is illustrated, that the present invention can be employed with other systems (*e.g.*, linear, orbital, *etc.*). Also, while a single wafer 850 and a single wafer carrier 860 are illustrated, it is to be appreciated that multiple wafer and/or wafer carrier systems can be employed in accordance with the present invention.

Fig. 9 illustrates an example CMP process. Again, such CMP processes are well known in the art and thus are discussed only briefly herein for brevity. A wafer 920, whereupon one or more features 930 have been fabricated, and upon which a metal film 940 has been deposited, is presented to a CMP system 900 that includes a pad 910 upon which a slurry 950 has been dispensed. While a metal film 940 is described in association with Fig. 9, it is to be appreciated that CMP of other layers (*e.g.*, polysilicon, dielectric) may be characterized by the present invention. The abrasive particles in the slurry 950 and/or pad 910 are employed to remove reaction products from the metal film 940, which facilitates planarizing the metal film 940 and/or the features 930.

In view of the exemplary systems shown and described above, methodologies that may be implemented in accordance with the present invention will be better appreciated with reference to the flow charts of Figs. 10, 11 and 13. While, for purposes of simplicity of explanation, the methodologies are shown and described as a series of blocks, it is to be understood and appreciated that the present invention is not limited by the order of the blocks, as some blocks may, in accordance with the present invention, occur in different orders and/or concurrently with other blocks from that shown and described herein. Moreover, not all illustrated blocks may be required to implement a methodology in accordance with the present invention.

Fig. 10 is a flow diagram illustrating one particular methodology 1000 for carrying out a characterization and/or CMP control in accordance with an aspect of the present invention. At 1010, general initializations occur. The initializations may include, but are not limited to, establishing data communications, establishing initial values, identifying communicating apparatus and/or processes and positioning CMP means and products, for example. At 1020, a test wafer is acquired. As described above, one or more electrical resistance member(s) and/or electrical resistance entities arranged in various patterns at various depths in diverse layers may be associated with the test wafer. CMP processes performed on test wafers of varying thickness, with different metal layers (*e.g.*, Cu, Ti, Ta, W, Al *etc.*), with different non-metal layers (*e.g.*, polysilicon, dielectric) with or without IC features may be characterized by the method 1000. While one characterization process may focus on a small set of wafers (*e.g.*, all Cu, same pattern, same depths), a different characterization process may employ a larger set of wafers (*e.g.*, Cu and Ti, different patterns, different depths) to

facilitate characterizing different CMP processes. At 1030, polishing the wafer begins. Information including, but not limited to wafer data, pad data, pressure data, motion data and/or slurry data, for example, may be recorded to facilitate creating relations that can be employed in characterizing the CMP process. At 1040, electrical resistance(s) are read from the test wafer -- it is to be appreciated that one or more electrical resistance(s) from one or more electrical resistance member(s) and/or electrical resistance entities may be read at 1040. Furthermore, it is to be appreciated that block 1040 may be performed substantially in parallel with block 1030. The electrical resistance(s) readings may be gathered, for example, continuously and/or at discrete time intervals. The electrical resistance information may include, but is not limited to, electrical resistance(s) of electrical resistance member(s) and/or entities embedded in a wafer before the CMP process, wafer electrical resistance(s) recorded during the chemical mechanical polishing process and the time associated with such reading, electrical resistance(s) recorded after revolutions of a polishing pad during the chemical mechanical polishing process and the number of revolutions associated with such reading, and electrical resistance(s) recorded after percentages of the layers have been removed during the chemical mechanical polishing process and the percentage removed associated with such reading. The electrical resistance(s) can be used to determine wafer stress(es).

At 1050, a determination is made concerning whether the CMP is complete. If the determination at 1050 is NO, then processing returns to 1030. While block 1050 is shown as a discrete block, separate from 1030 and 1040, it is to be appreciated that such blocks may be performed substantially in parallel. If the determination at 1050 is YES, then at 1060, information is stored. Such information can include, but is not limited to, electrical resistance information, slurry information, pad information, pressure information, motion information and polish data (*e.g.*, polish time, material removed, number of revolutions, *etc.*). At 1060, in addition to and/or alternatively, relations between the information described above may be stored. Such relations may be employed, for example, in subsequent characterization analyses that employ techniques including, but not limited to, data mining, database analysis, regression analysis, neural network processing, machine learning analyses and other analytical techniques. Thus, the CMP process can be characterized. Such characterization may include, but is not limited to, producing information concerning wafer electrical

resistance(s) as related to polishing rate, polishing uniformity, polishing time, polishing effects on pads, slurry usage and the introduction of defects to the wafer. Such characterization data can be employed, for example, to facilitate initializing production CMP runs to optimize such production runs by controlling wafer electrical resistance(s) and/or it may also be employed in controlling a CMP process.

At 1070 a determination is made concerning whether there is another wafer to polish during the CMP characterization process. If the determination at 1070 is NO, then processing can conclude, otherwise processing may return to 1020.

Fig. 11 is a flow diagram illustrating one particular methodology 1100 for carrying out a production run portion of the present invention that benefits from a characterization portion of the present invention like that described in association with Fig. 10. At 1110, general initializations occur. The initializations may include, but are not limited to, establishing data communications, establishing initial values, identifying communicating apparatus and/or processes and positioning chemical mechanical polishing means and products, for example.

At 1110, a production wafer is acquired. Such a production wafer may include IC features (*e.g.,* vias, lines, holes, *etc.*) and may include one or more metal layers and/or substrate layers. Based, at least in part, on information concerning the production wafer (*e.g.,* type of metal layer, thickness of layer, current planarity, desired planarity, ratio of up area to down area, *etc.*), and other information (*e.g.,* pad information, slurry information, pressure information, motion information), at 1130, initial CMP parameters may be retrieved. By way of illustration, during a characterization process, a relationship between wafer electrical resistance(s) and metal layer thickness, desired removal amount, desired removal rate and slurry formula, concentration and dispense rate may have been produced. Thus, rather than employ generic CMP parameters that may not produce desired wafer electrical resistance(s), a CMP apparatus and/or process may benefit from the relationship identified during the previous characterization process. Thus, at 1140, the CMP apparatus and/or process may be programmed based on such relationship and/or other retrieved data to facilitate achieving and/or maintaining desired wafer electrical resistance(s) (*e.g.,* wafer stress(es)). Based on such data, and on characterization data produced during a characterization phase, a slurry formula, concentration and dispense rate may be chosen that will increase the likelihood that a desired wafer stress(es) will

be achieved and thus that such polishing will be achieved, given the current state of the pad, for example.

At 1150, the wafer is polished and at 1160 a determination is made concerning whether there is another wafer to polish. If the determination at 1160 is NO, then processing may conclude, otherwise processing may return to 1120.

While Figs. 10 and 11 describe a bifurcated system, where characterization occurs and then production wafers are fabricated, Fig. 12 concerns a wafer 1200 with IC features 1210 and electrical resistance entities 1220 that can be employed, for example, by a method like that described in association with Fig. 13 to control a CMP process and/or to characterize a CMP process during production. Thus, Fig. 12 illustrates a wafer 1200 whereupon IC features 1210 have been fabricated. While six IC features 1210 are illustrated, it is to be appreciated that a greater and/or lesser number of such features may be present. Similarly, while three electrical resistance entities 1220 are illustrated, it is to be appreciated that a greater and/or lesser number of electrical resistance entities 1220 arranged in various patterns at various depths may be employed.

Fig. 13 is a flow diagram illustrating one particular methodology 1300 for carrying out *in-situ* monitoring, controlling and/or characterization of a CMP process. At 1310, general initializations occur. The initializations may include, but are not limited to, establishing data communications, establishing initial values, identifying communicating apparatus and/or processes and positioning chemical mechanical polishing means and products, for example.

At 1320, a production wafer is presented to the method 1300. Such a production wafer may include IC features (*e.g.,* vias, lines, holes, *etc.*) and may include one or more metal layers, polysilicon layers, dielectric layers and/or substrate layers and may also include one or more electrical resistance member(s), electrical resistance entities and/or associated electrical resistance-related equipment (*e.g.,* circuitry and/or power supply). Based, at least in part, on information concerning the production wafer (*e.g.,* type of layer, thickness of layer, current planarity, desired planarity, ratio of up area to down area, *etc.*), and other information (*e.g.,* electrical resistance information, pad information, slurry information, pressure information, motion information), at 1330, initial CMP parameters may be retrieved. Such parameters may be established to facilitate achieving and/or maintaining wafer

electrical resistance(s) (*e.g.*, wafer stress(es)) during CMP, which can facilitate achieving more precise chemical reactions in the CMP process. At 1340, the CMP apparatus and/or process may be programmed based on such relationship and/or other retrieved data. Based on such data, and on characterization data produced during a characterization phase, a slurry formula, concentration and dispense rate may be chosen that will increase the likelihood that desired wafer stress(es) will be achieved and/or maintained and thus that such desired polishing will be achieved. Such selections may be predicated on the resulting wafer electrical resistance(s) and reaction rate.

At 1350, the wafer is polished and at 1360 electrical resistance information is recorded from the wafer-based electrical resistance member(s) and/or electrical resistance entities. While blocks 1350 and 1360 are illustrated as discrete blocks, it is to be appreciated that blocks 1350 and 1360 may be performed substantially in parallel so that electrical resistance monitoring can occur while the CMP is in progress. The electrical resistance(s) can be used to determine wafer stress(es).

At 1370, a determination is made concerning whether the CMP is complete. If the determination at 1370 is YES, then processing can conclude, otherwise, processing may proceed to 1380. At 1380, a determination is made concerning whether desired polish parameters (*e.g.*, electrical resistance(s), time, rate, planarity, *etc.*) are being achieved by the CMP process. Such a determination may be based, for example, on electrical resistance(s) of the wafer. If the determination at 1380 is YES, then processing may return to 1350. But if the determination at 1380 is NO, then at 1390, one or more CMP parameters may be adjusted. By way of illustration and not limitation, CMP parameters including, but not limited to pressure, motion, speed, slurry dispense rate, and the like, may be adapted. By way of further illustration, if the desired rate of removal of the 0.50 μm of the titanium of 200 nm/min is not being met, for example, if only 100 nm/min is being achieved, then the slurry dispense rate, the speed and/or the pressure may be adapted in an attempt to increase the removal rate. Furthermore, if the removal rate is not being met, then pad reconditioning and/or replacement may be scheduled. Such adaptations are facilitated by the relationships between electrical resistance(s) and CMP factors as determined during a characterization process. In one example of the present invention, to facilitate

providing an up-to-date CMP characterization, the electrical resistance data monitored at 1360 may be employed to update the characterization data.

Described above are preferred embodiments of the present invention. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the present invention, but one of ordinary skill in the art will recognize that many further combinations and permutations of the present invention are possible. Accordingly, the present invention is intended to embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended claims.